CONDUCTIVE INTERCONNECTIONS THROUGH THICK SILICON SUBSTRATES FOR 3D PACKAGING

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ABSTRACT

We have developed key technologies to form conductive interconnections through a thick silicon substrate, which are potentially applied for 3D device fabrication or packaging of optical MEMS devices. In this paper, we demonstrate to form metal filled Through-Holes (THs) in thick Silicon (Si) substrates (t=~500μm) mainly using Photo Assisted Electro-Chemical Etching (PAECE)[1][2] and Molten Metal Suctioned Method (MMSM)[3]. The THs that we experimentally made with these technologies had 15μm in the diameter and the aspect ratio of 35. And the maximum density was 500THs/cm^2. The dielectric breakdown voltage of the THs was more than 500V. In the result of a radioisotope leak test using Kr-85, the leakage rate of THs between the front and the back of the substrate was lower than the detection limit (1 X 10^{-15} Pa•m^3/sec.).

INTRODUCTION

Forming conductive interconnections through silicon substrates is an essential technology for high-density packages, module assemblies and system integration. The interconnections are expected to give solutions to recent demands for downsizing and cost reduction of mobile phone or PDA fabrications.

Thinner back grinded wafers are typically used in high-density integrations, such as memory modules. Consequently, Deep-Reactive Ion Etching (DRIE), usually Inductively Coupled Plasma Reactive Ion Etching (ICP-RIE) is adopted, for Si TH forming, Plasma Enhanced-Chemical Vapor Deposition (PE-CVD) for insulator forming and electro or non-electro plating for metal interconnection can be applied with the help of the thinner Si substrate [4].

On the other hand, thicker wafers are preferred in Micro Optical Electro-Mechanical System (MOEMS), which isn't allowed to be grinded or polished for the backside of the substrate, or in Silicon Optical Bench (SiOB) on which the high heat generating laser diode is mounted. There are some obstacles to be overcome to form the conductive interconnections through Si due to the thick substrate.

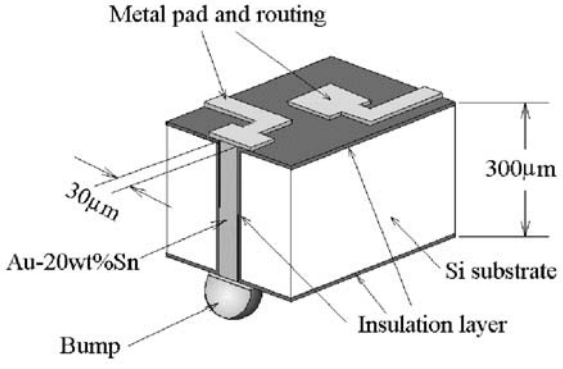

Figure 1 *Schematic illustration of conductive interconnections through silicon substrate*

Figure 1 shows schematic illustration of a target structure in our studies, which can be applied in optical devices. In this case, the thickness of Si substrate is 300μm and the diameter of the TH is 30μm (aspect ratio 10). When the metal filled THs are utilized for electrostatic actuators, a high dielectric breakdown voltage of the insulators against Si substrate is required. And moreover, the airtightness of conductive interconnections is very important for hermetic seal structures against humidity. To satisfy all these requirements, we proposed the PAECE and the MMSM to form the metal filled THs. The followings describe the principal, fabrication processes, experimental methods and evaluation results of these two key technologies. In addition, we also evaluated other alternative technologies to form the metal filled THs and compared the advantages and disadvantages among them in the discussion.

FABRICATION

The fabrication process that we have done to form the target interconnections consists of three major steps. The first one is formation of through-holes in a silicon substrate, and then forming process of insulation layer must be required. And finally, refilling the through-holes with conductive material makes electrical contact between the front and the back of Si substrate.

Forming TH

We mainly used PAECE to open THs in a silicon substrate, which is an anisotropic wet etching technology. Because TH formed by the method has a high aspect ratio (more than 100) and a good forthrightness (less than 0.5°). And it could be done with an inexpensive equipment. The PAECE requires pre and post process to make through-holes. Figure 2 shows the process flow, and Figure 3 shows the schematic illustration of the PAECE experiment system. The starting material was a n-type, 525μm thickness and double side mirror polished Si wafer, of which direction was (100) grown by the Magnetic Czochralski (MCZ). First, 110nm Si_3N_4 film layer was deposited by LP-CVD. Then, 30nm Cr and 500nm Au films were successively sputtered on Si_3N_4 layer. These metal layers work as protection masks against HF solution. At the same time, they keep uniformity of electrical field between anodic Si wafer and cathode Pt plate in the PAECE system. In order to make initial etch pits, Au/Cr and Si_3N_4 layers are selectively opened by a typical photolithography. V-grooves were formed from the opening by anisotropic etching with KOH solution. Typical PAECE conditions are;

- Current density: 6.0mA/cm^2 (DC voltage = 0.5-2.0V)

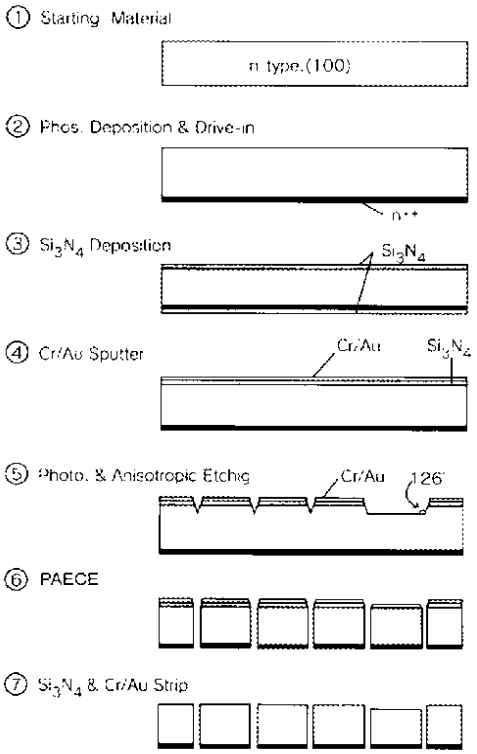

Figure 2 *Pre and post processes for PAECE*

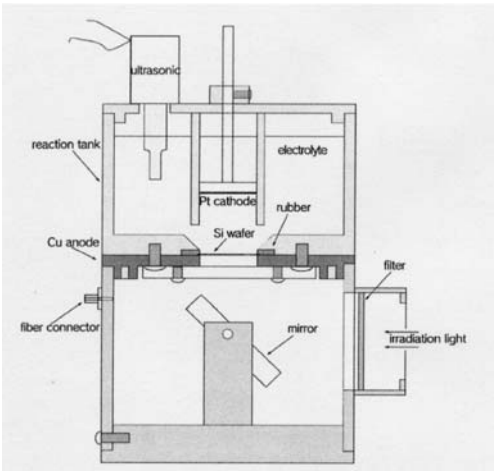

Figure 3 *Schematic illustration diagram of PAECE equipment system*

- Light intensity: 5.9mW/cm^2
- Electrolyte: 2.5wt% HF solution
- Surfactant: C_2H_5OH 10%
- Temperature of electrolyte: 50˚C

A Xenon lamp was used as the light source to irradiate the backside surface of the wafer, and a band-pass filter (from 370nm to 750nm of wavelength) was placed in the optical path. After the PAECE process, the protection, such as Si_3N_4 and Au/Cr films were stripped.

The followings and Figure 4 describe the mechanism of the PAECE. The minority carriers, positive holes in this case, are generated within a depth of approximately 11µm from the bottom surface. They move toward the front surface

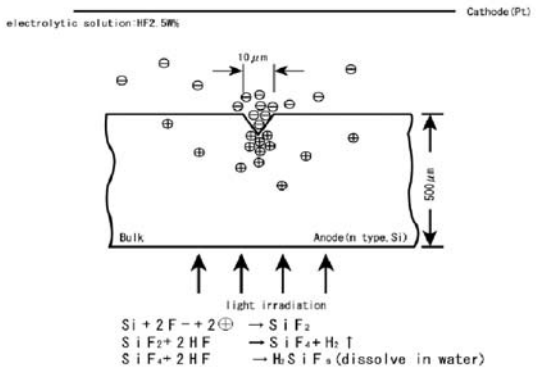

Figure 4 *Principle of PAECE*

by the electric field applied to the system. Where the V-groove exists on the front surface of the Si substrate, the electric field concentrates at the peak of the V-groove leading electric charges (positive holes). The chemical reaction as shown below occurs there, and only the certain points where it occurs are etched to form TH.

$$Si + 6HF + 2hole(+) \rightarrow H_2SiF_6 + H_2 + 2H^+ \qquad (1)$$

We succeeded to make 500THs/cm^2 in a thick Si substrate, each of which opening diameter was 15µm and the aspect ratio was 35. The etching rate was around 1.0µm/min. under the optimized conditions for good sidewall morphology of the TH. Figure 5 shows the cross-sectional views of the THs.

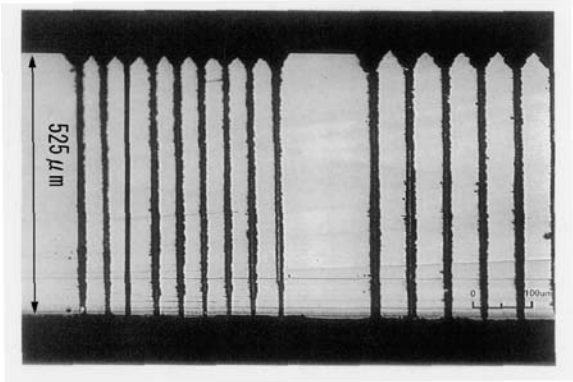

Figure 5 *Potogrape of Cross sectional view of THs made by PAECE*

Insulator Forming

After the THs forming, we put insulating layers on the sidewalls of THs and surface of the wafers. SiO_2 insulator was formed by thermal oxidation (1100˚C, 3 hours in steam).

The thickness of the SiO_2 layer on both the surface of substrate and the sidewall of the THs were 1.2µm, which was measured on cross sectional SEM photograph.

Metal Refilling

The MMSM we have proposed is a solution to fill very high aspect ratio through-holes with metal. Figure 6 shows

the process flow. In the experiments, the wafer was set in a chamber first, where was evacuated to 50Pa•abs., and then a melting bath was heated up to 330˚C in case of Au-20wt%Sn solder. The wafer formed THs and insulation layer was dipped in the bath after the metal melt completely. One minute after the dipping, N_2 gas was introduced to the chamber up to atmospheric pressure, and the chamber was pressurized to 200kPa by N_2 gas subsequently. After keeping the pressure for 1 minutes, the sample was taken out from the chamber checking if the remaining metal on the surface had solidified. The excessive metal was removed by wiping during reheating process or wet etching. To improve the yield rate of the filling, we spattered Cr (30nm) and Au (500nm) at the opening edges of THs. And the metal overflowed THs the openings and formed interconnection lands, which were defined by the Cr/Au pattern on the surface of the Si substrate.

Figure 7 shows the cross-section views of Sn buried inside the THs in a thick Si substrate. The THs sized 30μm in the opening diameter with the aspect ratio of 14 were completely filled without any voids. The forming process of THs was DRIE in this case.

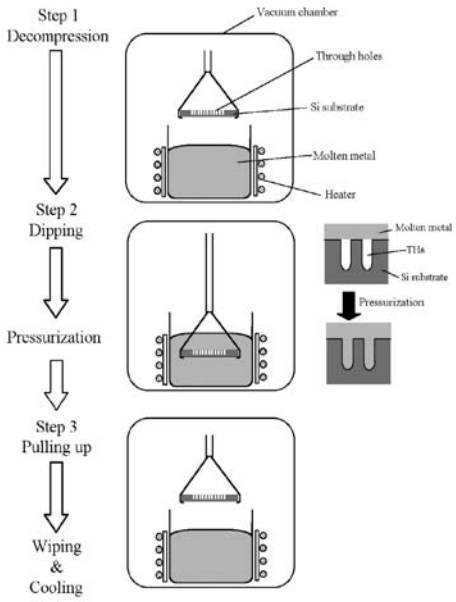

Figure 6 *Process flow of MMSM*

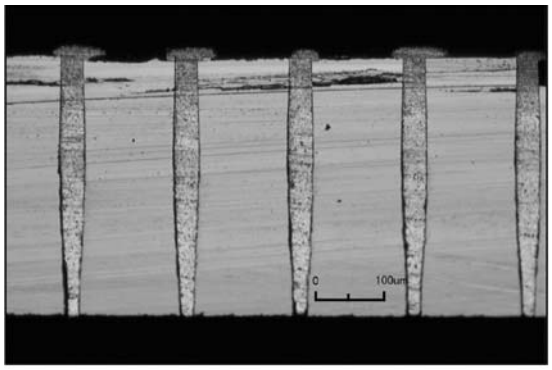

Figure 7 *Cross sectional view of metal filled THs*

EVALUATION

We evaluated the dielectric breakdown voltage of the metal filled THs as well as the leak rate between the top surface of the Si substrate and the bottom. The dielectric breakdown voltage was more than 500 volts. In the result of a radioisotope leak test using Kr-85, the leakage was lower than the detection limit (1 X 10^{-15} Pa•m^3/sec.).

DISCUSSION

In this discussion, we would like to compare our proposing technologies to other possible technologies.
DRIE or laser processes are typical techniques to make TH in Si substrate. DRIE is often used in fabrications for MEMS devices, which require complex structures, deep bulk anisotropic etching and a high speed-etching rate. However it has limitations in a deep etching as forming a high aspect ratio TH on the ground of the difficulties in supplying of etching species from the front opening to the bottom of the THs. In addition, the cross section shape of THs formed by DRIE is usually barrel one, which may make troubles in later processes. One of problems in laser processes forming is its rough quality of THs sidewall as it physically breaks Si. Others are derbies which are produced around openings and a smaller diameter of THs at the backside than the front the front openings'. And moreover, the tact time during a high-density process would be longer because each TH has to be formed one by one by a laser beam.

PAECE can make high aspect ratio THs, however the substrate must be n-type (100) and there are two major problems in its sidewall qualities. One is so-called 'side-branch', which is etching profile proceeding to a certain undesirable [010] and [001] directions. Figure 8 shows another cross sectional view of THs made by PAECE. While the sidewall in the [110] cutting plane have good morphology, the 'side-branches' are clearly observed in the [001] and [010] planes at THs made in the same substrate. The other is 'peripheral effect', which is a phenomenon that THs located at the edge of relatively high-density pattern have much more the 'side-branch'. We have improved the sidewall quality of THs to reduce the depth of the 'side-branch' and the 'peripheral effect'. Through some experiments, we finally concluded the

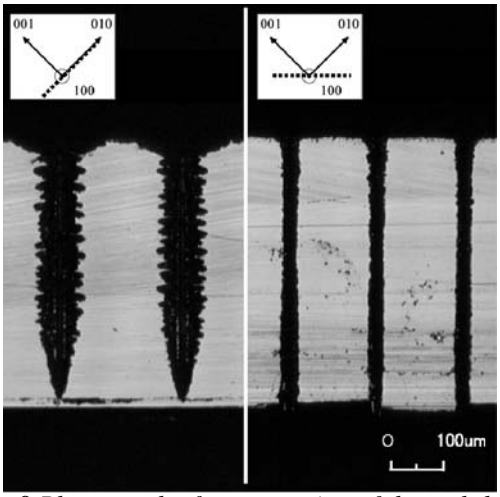

Figure 8 *Photograph of cross section of through-holes by PAECE. Broken lines mean cutting planes.*

reason why the 'side-blanches' were produced was that more dangling bonds of the [001] and [010] was attacked by HF solution and surplus holes compared to [110] direction's. In order to suppress the excessive holes, we used a silicon substrate that had a higher resistivity. Space Charge Region (SCR), which is defined by the following equation, would dominate the phenomenon.

$$d = [2\varepsilon\varepsilon_0(V_D\text{-}V)/eN_D]^{1/2} \qquad (2)$$

SCR in a high resistivity substrate is much wider than a lower resisitivity's. Since there are few carriers in SCR, the minority positive holes would hardly reach to the starting points of the 'side-branch'. The depth of the 'side-branches' in a 80~120Ω-cm substrate was 75% less than in a 1~2Ω-cm one. In addition, the narrower (80μm) TH pitch improved 13% of the depth compared to the wider (162.5μm) pitch. This also means that the narrower pitch restrict supplying holes to each TH, and suppress holes to work at undesired places. With regard to the 'peripheral effect', we assumed that other excessive holes generated by the backside lighting caused the phenomenon, which usually occurred in the edge THs of relatively high-density. In order to suppress it, we formed a sputtered Al shade mask at the back surface of the wafer, which has aligned small opening windows corresponding to the front V-groove positions vertically. In the experiment, the light intensity of the backside illumination was set to 49mW/cm^2, which was 50 times larger than that of no shade mask, because total opening area of the mask was a fiftieth of the full opened area. Figure 9 shows that the 'peripheral effect' was minimized to 79% with the shade mask.

Table 1 shows methods comparison for TH forming in thick Si substrates. We mainly use PAECE to open through-holes. At the same time, we experimentally made through-holes with other technologies, such as Deep RIE or laser processing, and evaluated pros and cons among them. When we apply these technologies in a high volume production, we have to consider the machine cost of each method as well.

We currently have used thermal oxidation for the insulator forming. However other low temperature processes up to 400˚C must be required when we have to handle IC built in Si substrates. The PE-CVD would be the most possible alternative technology, but it is difficult to form reliable and thick SiO_2 layers in deep THs at this moment.
We are considering to use Anodic oxidation for our alternative solution, which we can do at room temperature.

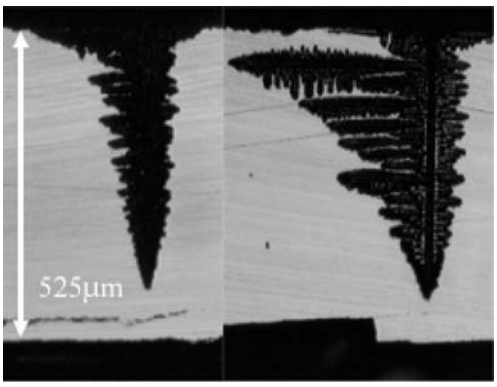

Figure 9 *Photograph of cross section of through-holes by PAECE with the backside mask shade (left), the 'peripheral effect' in fully opened backside (right).*

Table 1 Methods Comparison for TH Forming in Thick Si Substrates

Method	Source or Material	Min. Bore (μm)	Max. Depth (μm)	Throughput	Remarks
PAECE	Xenon	10	500	1.0μm/min.	n-type substrate only Side Branches
DRIE	SF_6	2	100	2.5μm/min.	Barrel shape
		50	500	>10μm/min.	
Laser processing (Abrasion)	YAG	55	530	3-5sec./hole	Debris Cone shape
	UV	20	700	80holes/sec.	
		>50	700	8holes/sec.	

Regarding methods for refilling THs with conductive material, electro or non-electroplating are typical techniques to form conductive interconnections in the THs. However, those methods cannot be applied for filling high aspect ratio THs due to the difficulties in circulation of the plating solution causing undesirable voids in the metal. Therefore, our MMSM have the advantage because of its capability to fill high aspect ratio THs without any voids. However, the selection of the filled metal for the MMSM must be considered as follows:
(1) Low vaporization pressure at the melting point to perform filling operation in vacuum
(2) Low coefficient of thermal expansion to prevent the sucked metal from forming voids due to shrinking during cooling
(3) Low resistivity of metal to make low impedance interconnection

Listed in Table 2 are several metals that we filled through-holes by MMSM in the experiments at this moment.

Table 2 Melting Point of Refilled Metal for MMSM

Metal	T_M (˚C)
In	156.4
Sn	231.9
Au-Sn20(wt%)	280.0

CONCLUSIVE SUMMARY

Conductive interconnections through thick Si substrate have been experimentally made using two newly developed technologies. As the forming processes of the through-holes, the Photo Assisted Electro-Chemical Etching (PAECE) has been applied and its 'side-branches' and 'peripheral effect' were improved by controlling substrate resistivity and surplus holes. And it was demonstrated that high aspect ratio THs were filled with a certain metal by the Molten Metal Suctioned Method (MMSM), which had enough dielectric breakdown voltage against the substrate (more than 500V) and no-leakage between the front and the back of the substrate (less than 1 X 10^{-15} Pa•m^3/sec.).

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